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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,894	08/28/2001	Christoph Dominique Loeffler-Lejeune	BAY-007	7829

7590 04/05/2006

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EXAMINER	
HAN, CLEMENCE S	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,894	LOEFFLER-LEJEUNE, CHRISTOPH DOMINIQUE	
	Examiner	Art Unit	
	Clemence Han	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment received on 01/09/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 13-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15 and 16* is/are allowed.

6)☒ Claim(s) *1-11,13,14,17-20 and 22-26* is/are rejected.

7)☒ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claim 1-11, 13, 14, 17-20 and 22-26 are rejected under 35 U.S.C. 102(a) as being anticipated by Sawey et al. (US Pub. 2002/0118668).

Regarding to claim 1, Sawey teaches an integrated circuit comprising: a first input port 850 a for receiving a first time-division multiplexed signal that comprises a first series of frame boundaries; a second input port 860 for receiving a second time-division multiplexed signal that comprises a second series of frame boundaries; a first frame position register (502 in 850) whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a point in time; and a second frame position register (502 in 860) whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said point in time.

Regarding to claim 2, Sawey teaches a first memory (506 in 850) that stores said first time-division multiplexed signal at a location that is indicated by a first write pointer (504 in 850) and that reads said first time-division multiplexed signal

at a location that is indicated by a first read pointer (508 in 850); and a second memory (506 in 860) that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer (504 in 860) and that reads said second time-division multiplexed signal at a location that is indicated by a second read pointer (508 in 860).

Regarding to claim 3, Sawey teaches a first retimer (516, 522 in 850) for retiming said first time-division multiplexed signal; and a second retimer (516, 522 in 860) for retiming said second time-division multiplexed signal.

Regarding to claim 4, Sawey teaches an output port 300; and a cross-connect 14 for outputting at least a portion of said first time-division multiplexed signal via said output port.

Regarding to claim 5, Sawey teaches a method comprising: receiving a first time-division multiplexed signal that comprises a first series of frame boundaries 850; receiving a second time-division multiplexed signal that comprises a second series of frame boundaries 860; indicating, at a point in time, how far said first time-division multiplexed signal is from a frame boundary (502 in 850); and indicating, at said point in time, how far said second time-division multiplexed signal is from a frame boundary (502 in 860).

Regarding to claim 6, Sawey teaches storing said first time-division

multiplexed signal into a first memory (506 in 850) at a location that is indicated by a first write pointer (504 in 850); reading said first time-division multiplexed signal from a location in said first memory that is indicated by a first read pointer (508 in 850); storing said second time-division multiplexed signal into a second memory (506 in 860) at a location that is indicated by a second write pointer (504 in 860); and reading said second time-division multiplexed signal from a location in said second memory that is indicated by a second read pointer (508 in 860).

Regarding to claim 7, Sawey teaches retiming (516, 522 in 850) said first time-division multiplexed signal in accordance with a clock signal 510; and retiming (516, 522 in 860) said second time-division multiplexed signal in accordance with said clock signal.

Regarding to claim 8, Sawey teaches an apparatus comprising: a first integrated circuit comprising: (i) a first input port 850 for receiving a first time-division multiplexed signal that comprises a first series of frame boundaries; (ii) a second input port 860 for receiving a second time-division multiplexed signal that comprises a second series of frame boundaries; (iii) a first frame position register (502 in 850) whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a point in time; and (iv) a second frame position register (502 in 860)

whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said point in time; and a second integrated circuit comprising a controller 516, 522 for reading the contents of said first frame position register and said second frame position register.

Regarding to claim 9, Sawey teaches a first memory (506 in 850) that stores said first time-division multiplexed signal at a location that is indicated by a first write pointer (504 in 850) and that reads said first time-division multiplexed signal at a location that is indicated by a first read pointer (508 in 850); and a second memory (506 in 860) that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer (504 in 860) and that reads said second time-division multiplexed signal at a location that is indicated by a second read pointer (508 in 860); and wherein said controller 516, 522 is further for storing a value in said first read pointer (508 in 850) based on the contents of said first frame position register and said second frame position register [0058].

Regarding to claim 10, Sawey teaches an output port 300; and a cross-connect 14 for outputting at least a portion of said first time-division multiplexed signal via said output port.

Regarding to claim 11, Sawey teaches a composite switch comprising: a first integrated circuit comprising: a first input port 850 for receiving a first time-division multiplexed signal that comprises a first series of frame boundaries; a first frame position register (502 in 850) whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a point in time; and a second integrated circuit comprising: a second input port 860 for receiving a second time-division multiplexed signal that comprises a second series of frame boundaries, and a second frame position register (502 in 860) whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said point in time; and a controller 516, 522 for reading the contents of said first frame position register and said second frame position register.

Regarding to claim 13, Sawey teaches a first memory (506 in 850) that stores said first time-division multiplexed signal at a location that is indicated by a first write pointer (504 in 850) and that reads said first time-division multiplexed signal at a location that is indicated by a first read pointer (508 in 850); and a second memory (506 in 860) that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer (504 in 860) and that

reads said second time-division multiplexed signal at a location that is indicated by a second read pointer (508 in 860).

Regarding to claim 14, Sawey teaches said controller 516, 522 is further for storing a value in said first read pointer (508 in 850) based on the contents of said first frame position register and said second frame position register [0058].

Regarding to claim 17, Sawey teaches a controller 516, 522 configured to synchronize the first and second time-division multiplexed signals in response to the contents of the first and second frame position registers [0067].

Regarding to claim 18, Sawey teaches the controller is configured to generate first and second offset values 518 in response to the contents of the first and second frame position registers.

Regarding to claim 19, Sawey teaches the controller is further configured to adjust first and second read pointers in response to the first and second offset values, respectively [0058].

Regarding to claim 20, Sawey teaches a controller configured to adjust the first and second read pointers in response to the contents of the first and second frame position registers in order to synchronize the first and second time-division multiplexed signals [0058], [0067].

Regarding to claim 22, Sawey teaches adjusting the first and second read pointers in response to the indications of how far the first and second time-division multiplexed signals are from their respective frame boundaries at said point in time [0058].

Regarding to claim 23, Sawey teaches a controller 516, 522 configured to synchronize the first and second time-division multiplexed signals in response to the contents of the first and second frame position registers [0067].

Regarding to claim 24, Sawey teaches the controller is configured to generate first and second offset values 518 in response to the contents of the first and second frame position registers and to adjust the first read pointers in response to the first offset values and the second read pointers in response to the second offset values [0058].

Regarding to claim 25, Sawey teaches a controller 516, 522 configured to synchronize the first and second time-division multiplexed signals in response to the contents of the first and second frame position registers [0067].

Regarding to claim 26, Sawey teaches the controller is configured to generate first and second offset values 518 in response to the contents of the first and second frame position registers and to adjust the first read pointers in response

to the first offset values and the second read pointers in response to the second offset values [0058].

Response to Arguments

3. Applicant's arguments with respect to claim 1-13 and 15-17 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

4. Claim 15 and 16 are allowed.

5. Claim 21 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of the art with respect to the invention in general.

U.S. Patent 5,825,821 to Okuyama

U.S. Patent 6,067,304 to Nishioka

U.S. Patent 6,535,479 to van Heyningen et al.

U.S. Patent 6,970,480 to Ikematsu

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clemence Han whose telephone number is (571) 272-3158. The examiner can normally be reached on Monday-Thursday 7 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. H.

Clemence Han
Examiner
Art Unit 2616

STEVEN NGUYEN
PRIMARY EXAMINER